UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,796	03/23/2004	Martin Langhammer	15114H-073600US	4384

26059   7590   08/05/2008
TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER
YAARY, MICHAEL D

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
08/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/807,796	LANGHAMMER, MARTIN
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>28 May 2008</u>.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-32</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-32</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-32 are pending in the application.

Continued Examination Under 37 CFR 1.114

2.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on

05/28/2008 has been entered.

Claim Rejections - 35 USC § 101

3.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

4.   Claims 1-32 are rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter.

(i)   Claims 1 and 26 are directed to an apparatus; however, the claimed limitations

appear to be software per se, as the unit can be interpreted to be merely software. Thus

the claims are lacking any structural or hardware components comprising the

apparatus.

(ii)   Claims 2-13 and 27-32 are rejected for similar reasons as discussed for their
respective parent claims, as they fail to present any limitations that resolve the
deficiencies of the claims from which the depend.

(iii)   Claims 1, 14, and 26 are directed to an apparatus and method that merely
perform calculations and manipulation of data. In order for such a claimed invention to
be statutory, the claimed invention must accomplish a practical application. That is the
claimed invention must transform an article or physical object to a different state or
thing, or produce a useful, concrete, and, and tangible result; see State Street 47,
USPQ2d. It is clear from independent claims 1, 14, and 26 that the claimed invention
merely involves calculations and manipulations of data; that is multiplication of N-bit
numbers. The result produced by the invention, as recited in the claims, does not have
a real world value but merely a number without a practical application that makes the
result useful, concrete, and tangible. Therefore, independent claims 1, 14, and 26 are
directed to non-statutory subject matter as the claimed invention fails to accomplish a
practical application.

(iv)   Claims 2-13, 15-25, and 27-32 are rejected for similar reasons as discussed for
their respective parent claims, as they fail to present any limitations that resolve the
deficiencies of the claims from which the depend.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6.   Claims 1-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

(i)   Independent claims 1, 14, and 26 recite the limitation "...without summing any intermediate results." It is unclear based on the specification as to how the multiplication in the second mode is done without intermediate summation as the invention appears to store the partial words in different registers for multiplying. Thus it is unclear according to the specification how the 4N-bit result is formed without partial product summation.

(ii)   Claims 2-13, 15-25, and 27-32 are rejected for similar reasons as discussed for their respective parent claims, as they fail to present any limitations that resolve the deficiencies of the claims from which the depend.

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8.   Claims 1-6, 11-19, 24-27, and 31-32 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Moyse (US Pat. 5,446,651) in view of Yu (6,523,055) and Lee

et al. (hereafter Lee)(US Pat. 5,579,253).

9.   Yu was cited in the previous action dated 01/30/2008.

10..   **As to claims 1 and 14,** Moyse discloses a multiplication unit, comprising a 2N-

bit multiplier and having a first short word length multiplication mode and a second long

word length multiplication mode, wherein a short word length is N and a long word

length is 2N, wherein N is an integer (abstract), and wherein:

        In the first mode for multiplying two N-bit numbers, a first long word length

multiplicand and a second long word length multiplicand are multiplied together using

the 2n-bit multiplier to form a 4N-bit result (column 5, lines 26-41);

        in the second mode for multiplying two 2N-bit numbers, wherein a third long word

length is multiplicand is formed from a first pair of short word length words and a fourth

long word length multiplicand is formed from a second pair of short word length words

and subsequently the third and fourth long word length multiplicands are multiplied

together using the 2N-bit multiplier to form a 4N-bit result (column 5, lines 26-41).

11.   Moyse does not disclose that in the first mode, a first long word length
multiplicand is formed from a first short word length multiplicand, and a second long
word length multiplicand is formed from a second short word length multiplicand.

        However, in an analogous art, Yu discloses a first long word length multiplicand
is formed from a first short word length multiplicand, and a second long word length
multiplicand is formed from a second short word length multiplicand (Column 6, line 54-
column 7, line 7 disclose a multiplier circuit in which multiplicands generate intermediate
products wherein sign extension and zeroing are performed to properly align inputs for
multiplication. Thus, analogously, these extending techniques may be implemented in
the teachings of Moyse, to extend two N bit short words into long word lengths).

12.   Therefore, it would have been obvious to one of ordinary skill in the art at the
time of the invention, to modify the teachings of Moyse, by extending and zeroing
multiplicands in a multiplication circuit, as taught by Yu, for the benefit of effectively
aligning two N-bit multiplicands in a first multiplication state.

13.   The combination of Moyse and Yu do not disclose first words of the first and
second pairs of short word length words are stored in respective registers connected to
the 2N-bit multiplier and the multiplication is done without summing any intermediate
results.

        However Lee discloses first words of the first and second pairs of short word
length words are stored in respective registers connected to the 2N-bit multiplier and the

multiplication is done without summing any intermediate results (Figure 2; abstract; and column 2, line 56-column 3, line 12 disclose bit multiplication utilizing registers to store partial bit results.).

14.   Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Moyse and Yu, by multiplying and storing in respective registers partial bits of the multiplication data, as taught by Lee, in order to see increased performance benefits. Motivation to combine may be found in that the combination would allow for more time and instruction efficiency.

15.   **As to claim 26,** the claim is rejected for the same reasons as claim 1 and 14 above.

16.   **As to claims 2 and 15,** the combination of Moyse and Yu disclose in the first mode, the first long word length multiplicand is formed as a sign extended version of the first short word length multiplicand, and the second long word length multiplicand is formed as a sign extended version of the second short word length multiplicand (Yu, column, 6, lines 54-58 disclose sign extension of a multiplicand, but not necessarily performed on both multiplicands. However, it would have been obvious to one of ordinary skill in the art to apply sign extension to the multiplicands as necessary for correct aligning.).

17.   **As to claims 3 and 16,** the combination of Moyse and Yu disclose in the first

mode, the first long word length multiplicand is formed from the first short word length

multiplicand plus zeroes as the most significant bits, and the second long word length

multiplicand is formed from the second short word length multiplicand plus zeroes as

the most significant bits, such that the multiplication result includes an unsigned product

of the first and second short word length multiplicands (Yu, column 6, lines 54-58

disclose sign-extension performed, but does not explicitly disclose the sign-extending

includes adding zeroes to the most significant bits. However, it is well-known knowledge

in the art, that sign-extension on binary values is done by adding zeroes the most

significant bits to increase the number of bits of a binary number. Thus, it would have

been obvious to one of ordinary skill in the art to apply zeroes as the most significant

bits of the first and second short word lengths as necessary, to correct aligning.).

18.   **As to claims 4 and 17,** the combination of Moyse and Yu disclose in the first

mode, the first long word length multiplicand is formed from the first short word length

multiplicand plus zeroes as the least significant bits, and the second long word length

multiplicand is formed from the second short word length multiplicand plus zeroes as

the least significant bits, such that the upper bits of the multiplication result contain the

product of the first and second short word length multiplicands (Yu, column 6, lines 58-

61 disclose zeroing least significant bits of a multiplicand, but not necessarily performed

on both multiplicands. However, it would have been obvious to one of ordinary skill in

the art to apply zeroing to the multiplicands as necessary for correct alignment.).

19.   **As to claims 5 and 18,** the combination of Moyse and Yu disclose in the second

mode, second words of the first and second pairs of short word length words are stored

in respective registers, before the third and fourth long word length multiplicands are

multiplied together (Moyse, column 12, line 65-column 13, line 13 discloses registers in

a hardware floating point calculation unit, thus storing the necessary values used in the

circuit for multiplying.).

20.   **As to claims 6 and 19,** the combination of Moyse and Yu disclose a register file,

from which the first and second short word length multiplicands, and the first and

second pairs of short word length words, can be retrieved (Moyse, column 12, line 65-

column 13, line 13).

21.   **As to claim 27,** the combination of Moyse and Yu disclose in the second mode

of operation, the fifth and sixth data words of the first length are stored in respective

multiplication registers after retrieval from the register file (Moyse, column 12, line 65-

column 13, line 13).

22.   **As to claims 11, 12, 24, 25, 31 and 32,** the combination of Moyse and Yu

disclose the short word length is 16 bits or 18 bits, and the long word length is 32 or 36

bits (Moyse, abstract discloses a 2n multiplier for multiplication of n and 2n bits. Thus, it

would have been obvious to one of ordinary skill in the art at the time of the invention to

utilize any range of n bits and 2n bits accordingly as can fit in the data memory.).

23.   **As to claim 13,** the claim is rejected for the same reasons as claims 1 and 3

above.

24.   Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Moyse in view of Yu and Lee as applied to claims 6 and 19 above, and further in view of

Henderson et al. (hereafter Henderson)(US Pat. 6,484,194).

25.   Henderson was cited in the previous action dated 01/30/2008.

26.   **As to claims 7 and 20,** the combination of Moyse, Yu and Lee do not disclose

the register file is a dual ported register file, such that:

In the first mode, the first and second short word length multiplicands can be

retrieved at the same time, and in the second mode, first words of the first and second

pairs of short word length words can be retrieved at a first time, and second words of

the first and second pairs of short word length words can be retrieved at a second time.

However, Henderson discloses a dual ported register file (column 13, lines 39-

44), such that:

In the first mode, the first and second short word length multiplicands can be

retrieved at the same time, and in the second mode, first words of the first and second

pairs of short word length words can be retrieved at a first time, and second words of

the first and second pairs of short word length words can be retrieved at a second time

(Column 13, lines 39-61 and figure 5b disclose a multiplication circuit utilizing dual

ported registers to access data in different cycles. Thus, when combined with the

teachings of Moyse, Yu and Lee, may be implemented to read different word sets and

the same or different times.

27.   Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to modify the teachings of Moyse , Yu and Lee, by implementing a

dual ported register file, as taught by Henderson, for the benefit of maintaining fast

execution time in the multiplier circuit.

28.   Claims 8-10, 21-23, and 28-30 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Moyse in view of Yu and Lee as applied to claims 1, 14, and 26

above, and further in view of Bosshart (US Pat. 4,754,421).

29.   Bosshart was cited in the previous action dated 01/30/2008.

30.   **As to claims 8, 21 and 28,** the combination of Moyse, Yu and Lee do not

disclose first and second long word length accumulators, for receiving the multiplication

results.

However, in an analogous art, Bosshart discloses first and second long word

length accumulators, for receiving the multiplication results (Column 3, lines 2-8 and

figure 1 disclose accumulators A and B receiving multiplication results, and when

combined with the teachings of Moyse, Yu and Lee, can be implemented as long word

length accumulators accordingly.).

31.   Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to modify the teachings of Moyse, Yu and Lee, by implementing

first and second accumulators, as taught by Bosshart, for the benefit of immediately

being able to store multiplication results.

32.   **As to claims 9, 22, and 29,** the combination of Moyse, Yu, Lee and Bosshart

disclose in the second mode, the result of multiplying together third and fourth long word

length multiplicands can be divided between the first and second long word length

accumulators (Bosshart, column 4, lines 25-54).

33.   **As to claims 10, 23, and 30,** the combination of Moyse, Yu, Lee and Bosshart

disclose in the second mode, a selected part of the result of multiplying together the

third and fourth long word length multiplicands can be stored in a selected one of the

first and second long word length accumulators (Bosshart, column 4, lines 25-54).

Response to Arguments

34.   Applicant's arguments with respect to claims 1-32 have been considered but are

moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL YAARY whose telephone number is

(571)270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m -

5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193